IN THE CLAIMS

Please amend claims 2, 11 and 20, and add claims 28-30 as follows:

1.(Original) In a communications system including a receiver device for receiving symbols communicated via a communications channel and encoded according to a Complementary Code Key (CCK) chip encoding scheme, a system for decoding received CCK encoded symbols (chips), said system comprising:

a decision feedback equalizer (DFE) structure for receiving and equalizing CCK-encoded symbols communicated over a communications channel, and providing an output comprising an estimation of said received symbols, said DFE structure including a forward equalizer path and a feedback equalizer path including a feedback filter;

a CCK decoder means embedded in said feedback path and operating in conjunction with a feedback filter therein for decoding said chips, said decoding of CCK chips being based on intermediate DFE outputs including those chips corresponding to past decoded CCK symbols,

wherein decisions on a symbol chip at a particular time are not made until an entire CCK codeword that the chip belongs to is

decoded, thereby reducing errors propagated when decoding said symbols.

2. (Currently Amended) The system according to Claim 1, wherein the decoding and equalization are performed on a block of eight 8 chips of said intermediate DFE outputs ($\tilde{c}_{k+j}$) for CCK modes.

3. (Original) The system according to Claim 2, wherein estimated DFE equalizer outputs $\tilde{c}_{k+j}$ for CCK mode symbols is governed according to the equation:

$$\tilde{c}_{k+j} = s_{k+j} + \sum_{i=1}^{j} b_i c_{k+j-i}, \text{ where } s_{k+j} = \sum_{i=0}^{L_f-1} f_i r_{2(k+j)+d_f-i} + \sum_{i=j+1}^{L_b} b_i \hat{c}_{k+j-i}$$

j=0,...7 and represents the intermediate DFE equalizer outputs that include, in the feedback filter, only those chips corresponding to past decoded CCK symbols, f_i are forward equalizer taps, b_i are feedback equalizer taps, r_k represents a received input stream at a specified rate, L_f represents a length of the forward filter, d_f represents a delay through the forward filter, L_b represents a length of the feedback filter, and $\hat{c}_k$ represents a slicer output which is an estimate of the true transmitted chip c_k.

and the $\sum_{i=1}^{j} b_i c_{k+j-i}$ component represents the chips comprising the present transmitted symbol.

4.(Original) The system according to Claim 3, wherein the CCK decoder includes means for choosing from a set of possible CCK codewords, a codeword $\underline{c}$ = $[c_0, c_1, \ldots, c_7]$ that minimizes a metric comprising:

$$\sum_{j=0}^{7} \left| s_{k+j} + \sum_{i=1}^{j} b_i c_{j-i} - c_j \right|^2 .$$

5.(Original) The system according to Claim 4, wherein the codeword $\underline{c}$ is represented in terms of variables α_i and $\varnothing_1$ according to

$\underline{c}$ = $e^{j\phi 1}\underline{d}$ where $\underline{d}$ $\left[e^{j\alpha 1}, e^{j\alpha 2}, e^{j\alpha 3}, -e^{j(\alpha 2+\alpha 3-\alpha 1)}, e^{j(2\alpha 1-\alpha 2-\alpha 3}, e^{j(\alpha 1-\alpha 3)}, -e^{j(\alpha 1-\alpha 2)}, 1 \right]$

and each of α_i comprises one of four (4) values $[0, \pi/2, \pi, 3\pi/2]$, whereby $\underline{d}$ belongs to a set of 64 possible state vectors, and $\underline{c}$ may have 256 possible values.

6. (Original) The system according to Claim 5, wherein the CCK decoder includes trellis decoding means for generating a trellis structure having a plurality of trellis paths representing possible states of said codeword c, wherein a state in the trellis structure is represented by the vector [α_1, α_2, α_3].

7. (Original) The system according to Claim 6, wherein said metric to be minimized is governed according to:

$$\sum_{j=0}^{7}\left|\chi_j\right|^2 + 2\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7} s^*_{k+j}\chi_j\right] \text{ where } \chi_j = \sum_{i=0}^{j} b_i d_{j-i}..$$

8. (Original) The system according to Claim 7, wherein the metric to be minimized is governed according to

$\sum_{j=0}^{7} m_1(j) + 2\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7} m_2(j)\right]$ where $m_1(j) = \left|\chi_j\right|^2$ and is a real-valued quantity, and $m_2(j) = s^*_{k+j}\chi_j$ and is a complex-valued quantity, said trellis decoder structure including means for processing a block of eight (8) intermediate output symbols s_{k+j}, j = 0, 1,...,7, including means for calculating, at each time, j, for each branch in a trellis path, said $m_1(j)$ and $m_2(j)$ quantities; and, means for adding $m_1(j)$ and $m_2(j)$ quantities to the corresponding quantities of

the state from which the trellis branch originated, whereby the eight intermediate outputs $s_{k+j,}$ j = 0, 1,...,7, are processed by the trellis to determine the transmitted codeword at time k.

9.(Original) The system according to Claim 8, wherein said calculating means includes calculating, for each codeword state, the $\sum_{j=0}^{7} m_1(j) + 2\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7} m_2(j)\right]$ metric for each of four φ_1 values $[0, \pi/2, \pi, 3\pi/2]$, said means further choosing a state vector [α_1, α_2, α_3] and φ_1 that results in the minimum metric and calculating the transmitted codeword $\underline{c}$ accordingly therefrom, wherein a dimensionality of said trellis decoding means is reduced from 256 to 64.

10.(Currently Amended) A method for decoding symbols encoded according to a Complementary Code Key (CCK) chip encoding scheme, said method comprising the steps of:

a) providing a decision feedback equalizer (DFE) structure for receiving and equalizing CCK-encoded symbols (chips) communicated over a communications channel, said DFE structure further estimating said received symbols for DFE output, said DFE structure including a forward equalizer path and a feedback equalizer path

including a feedback filter;

b) embedding a CCK decoder means in said feedback path for decoding said chips in conjunction with filter taps ~~of~~ determined for said feedback filter; and,

c) decoding of said CCK chips based on intermediate DFE outputs including those chips corresponding to past decoded CCK symbols,

wherein decisions on a symbol chip at a particular time are not made until an entire CCK codeword that the chip belongs to is decoded, thereby reducing errors propagated when decoding said symbols.

11. (Currently Amended) The method according to Claim 10, wherein the decoding and equalization steps are performed on a block of eight 8 chips of said intermediate DFE outputs ($\tilde{c}_{k+j}$) for CCK modes.

12. (Original) The method according to Claim 11, wherein said estimating step includes calculating estimated DFE equalizer outputs $\tilde{c}_{k+j}$ for CCK mode symbols according to:

$$\tilde{c}_{k+j} = s_{k+j} + \sum_{i=1}^{j} b_i c_{k+j-i}, \text{ where } s_{k+j} = \sum_{i=0}^{L_f-1} f_i r_{2(k+j)+d_f-i} + \sum_{i=j+1}^{L_b} b_i \hat{c}_{k+j-i} \quad j=0,\ldots 7$$

and represents the intermediate DFE equalizer outputs that include, in the feedback filter, only those chips corresponding to past decoded CCK symbols, f_i are forward equalizer taps, b_i are feedback equalizer taps, r_k represents a received input stream at a specified rate, L_f represents a length of the forward filter, d_f represents a delay through the forward filter, L_b represents a length of the feedback filter, and $\hat{c}_k$ represents a slicer output which is an estimate of the true transmitted chip c_k, and the $\sum_{i=1}^{j} b_i c_{k+j-i}$ component represents the chips comprising the present transmitted symbol.

13.(Original) The method according to Claim 12, further including the step of: choosing from a set of possible CCK codewords, a codeword $\underline{c} = [c_0, c_1, \ldots, c_7]$ that minimizes a metric comprising:

$$\sum_{j=0}^{7} \left| s_{k+j} + \sum_{i=1}^{j} b_i c_{j-i} - c_j \right|^2 .$$

14.(Original) The method according to Claim 13, wherein the

codeword c̲ is represented in terms of variables $_{i}$ and $\emptyset_1$ according to $\underline{c} = e^{j\phi 1}\underline{d}$ where $\underline{d} = \left[e^{j\alpha 1}, e^{j\alpha 2}, e^{j\alpha 3}, -e^{j(\alpha 2+\alpha 3-\alpha 1)}, e^{j(2\alpha 1-\alpha 2-\alpha 3}, e^{j(\alpha 1-\alpha 3)}, -e^{j(\alpha 1-\alpha 2)}, 1\right]$ and each of α_i comprises one of four (4) values $[0, \pi/2, \pi, 3\pi/2]$, whereby $\underline{d}$ belongs to a set of 64 possible vectors, and c̲ may have 256 possible values.

15.(Original) The method according to Claim 14, wherein said decoding step c) further includes the step of generating a trellis structure having a plurality of trellis paths representing possible states of said codeword c̲, wherein a state in the trellis structure is represented by the vector $[\alpha_1, \alpha_2, \alpha_3]$.

16.(Original) The method according to Claim 15, wherein said metric to be minimized is governed according to:

$$\sum_{j=0}^{7}\left|\chi_j\right|^2 + 2\,\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7} s^*{}_{k+j}\chi_j\right] \text{ where } \chi_j = \sum\nolimits_{i=0}^{j} b_i d_{j-i}. .$$

17.(Original) The method according to Claim 16, wherein the metric to be minimized is governed according to

$\sum_{j=0}^{7} m_1(j) + 2\,\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7} m_2(j)\right]$ where $m_1(j) = \left|\chi_j\right|^2$ and is a real-valued

quantity, and $m_2(j) = s^*_{k+j}\chi_j$ and is a complex-valued quantity, said trellis generating step further including the steps of:

processing a block of eight (8) intermediate output symbols $s_{k+j,}$ j = 0, 1,...,7, including means for calculating, at each time, j, for each branch in a trellis path, said $m_1(j)$ and $m_2(j)$ quantities; and,

adding said $m_1(j)$ and $m_2(j)$ quantities to the corresponding quantities of the state from which the trellis branch originated, whereby the eight intermediate outputs $s_{k+j,}$ j = 0, 1,...,7, are processed by the trellis to determine the transmitted codeword at time k.

18.(Original) The method according to Claim 17, wherein the calculating step further includes the steps of:

calculating, for each codeword state, the $\sum_{j=0}^{7} m_1(j) + 2\,\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7} m_2(j)\right]$ metric for each of four φ_1 values $[0, \pi/2, \pi, 3\pi/2]$; and,

choosing a state vector $[\alpha_1, \alpha_2, \alpha_3]$ and φ_1 that results in the minimum metric and calculating the transmitted codeword <u>c</u> accordingly therefrom, wherein a dimensionality of said trellis structure is reduced from 256 to 64.

19.(Original) A receiver device for receiving symbols communicated via a communications channel, said symbols encoded according to a Complementary Code Key (CCK) chip encoding scheme, said receiver device comprising:

a decision feedback equalizer (DFE) structure for receiving and equalizing CCK-encoded symbols (chips) communicated over a communications channel, and providing an output comprising an estimation of said received symbols, said DFE structure including a forward equalizer path and a feedback equalizer path including a feedback filter;

a CCK decoder means embedded in said feedback path and operating in conjunction with a feedback filter therein for decoding said chips, said decoding of CCK chips being based on intermediate DFE outputs including those chips corresponding to past decoded CCK symbols,

wherein decisions on a symbol chip at a particular time are not made until an entire CCK codeword that the chip belongs to is decoded, thereby reducing errors propagated when decoding said symbols.

20. (Currently Amended) The receiver device according to Claim 19, wherein the decoding and equalization are performed on a block of eight 8 chips <u>of said intermediate DFE outputs ($\tilde{c}_{k+j}$)</u> for CCK modes.

21. (Original) The receiver device according to Claim 20, wherein estimated DFE equalizer outputs $\tilde{c}_{k+j}$ for CCK mode symbols is governed according to the equation:

$$\tilde{c}_{k+j} = s_{k+j} + \sum_{i=1}^{j} b_i c_{k+j-i}\ , \quad \text{where } s_{k+j} = \sum_{i=0}^{L_f-1} f_i r_{2(k+j)+d_f-i} + \sum_{i=j+1}^{L_b} b_i \hat{c}_{k+j-i} \quad j=0,\ldots 7$$

and represents the intermediate DFE equalizer outputs that include, in the feedback filter, only those chips corresponding to past decoded CCK symbols, f_i are forward equalizer taps, b_i are feedback equalizer taps, r_k represents a received input stream at a specified rate, L_f represents a length of the forward filter, d_f represents a delay through the forward filter, L_b represents a length of the feedback filter, and $\hat{c}_k$ represents a slicer output which is an estimate of the true transmitted chip c_k, and the $\sum_{i=1}^{j} b_i c_{k+j-i}$ component represents the chips comprising the present transmitted symbol.

22. (Original) The receiver device according to Claim 21, wherein the CCK decoder includes means for choosing from a set of possible CCK codewords, a codeword $\underline{c} = [c_0, c_1, \ldots, c_7]$ that minimizes a metric comprising:

$$\sum_{j=0}^{7} \left| s_{k+j} + \sum_{i=1}^{j} b_i c_{j-i} - c_j \right|^2 .$$

23. (Original) The receiver device according to Claim 22, wherein the codeword $\underline{c}$ is represented in terms of variables $_i$ and $\varnothing_1$ according to $\underline{c} = e^{j\phi 1}\underline{d}$ where $\underline{d}$ $= \left\lfloor e^{j\alpha 1}, e^{j\alpha 2}, e^{j\alpha 3}, -e^{j(\alpha 2+\alpha 3-\alpha 1)}, e^{j(2\alpha 1-\alpha 2-\alpha 3}, e^{j(\alpha 1-\alpha 3)}, -e^{j(\alpha 1-\alpha 2)}, 1 \right\rfloor$

and each of α_i comprises one of four (4) values $[0, \pi/2, \pi, 3\pi/2]$, whereby $\underline{d}$ belongs to a set of 64 possible vectors, and $\underline{c}$ may have 256 possible values.

24. (Original) The receiver device according to Claim 23, wherein the CCK decoder includes trellis decoding means for generating a trellis structure having a plurality of trellis paths

representing possible states of said codeword c̲, wherein a state in the trellis structure is represented by the vector [α_1, α_2, α_3].

25.(Original) The receiver device according to Claim 24, wherein said metric to be minimized is governed according to:

$$\sum_{j=0}^{7}\left|\chi_j\right|^2+2\,\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7}s^{*}{}_{k+j}\chi_j\right] \text{ where } \chi_j = \sum_{i=0}^{j} b_i d_{j-i}.\,.$$

26.(Original) The receiver device according to Claim 25, wherein the metric to be minimized is governed according to

$$\sum_{j=0}^{7}m_1(j)+2\,\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7}m_2(j)\right]$$

where $m_1(j)=\left|\chi_j\right|^2$ and is a real-valued quantity, and $m_2(j)=s^{*}{}_{k+j}\chi_j$ and is a complex-valued quantity, said trellis decoder structure including means for processing a block of eight (8) intermediate output symbols $s_{k+j,}$ j = 0, 1,...,7, including means for calculating, at each time, j, for each branch in a trellis path, said $m_1(j)$ and $m_2(j)$ quantities; and, means for adding $m_1(j)$ and $m_2(j)$ quantities to the corresponding quantities of the state from which the trellis branch originated, whereby the eight intermediate outputs $s_{k+j,}$ j = 0, 1,...,7, are processed by the trellis to determine the transmitted codeword at time k.

27. (Original) The receiver device according to Claim 26, wherein said calculating means includes calculating, for each codeword state, the $\sum_{j=0}^{7} m_1(j) + 2\mathrm{Re}\left[e^{j\phi 1}\sum_{j=0}^{7} m_2(j)\right]$ metric for each of four φ_1 values $[0, \pi/2, \pi, 3\pi/2]$, said means further choosing a state vector $[\alpha_1, \alpha_2, \alpha_3]$ and φ_1 that results in the minimum metric and calculating the transmitted codeword $\underline{c}$ accordingly therefrom, wherein a dimensionality of said trellis decoding means is reduced from 256 to 64.

28. (New) The system according to Claim 1, wherein the CCK decoder includes a trellis decoder having a number of trellis paths, wherein said number of trellis paths is less than all possible states of said entire CCK codeword that the chip belongs to.

29. (New) The method according to Claim 10, wherein said decoding step c) further includes the step of generating a trellis structure having a number of trellis paths, wherein said number of trellis paths is less than all possible states of said entire CCK codeword that the chip belongs to.

30. (New) The receiver device according to Claim 19, wherein the CCK decoder includes a trellis decoder having a number of trellis paths, wherein said number of trellis paths is less than all possible states of said entire CCK codeword that the chip belongs to.